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(58) Field of search
H1K
Selected US specifications from IPC sub-class H01L

(54) Buried interconnect for silicon on insulator structure

(57) To form an interconnect in a process where a recrystallized polysilicon layer 26 is formed over an insulating layer 20 a doped region 12 is formed in the substrate 10 prior to deposition of the polysilicon layer. The polysilicon layer 26 is in contact with at least a portion of the doped region 12 through an opening in the insulative layer 20. Recrystallization takes place through this opening, and, the doped region is electrically connected to a source or drain region of a semiconductor device formed in the recrystallized layer.

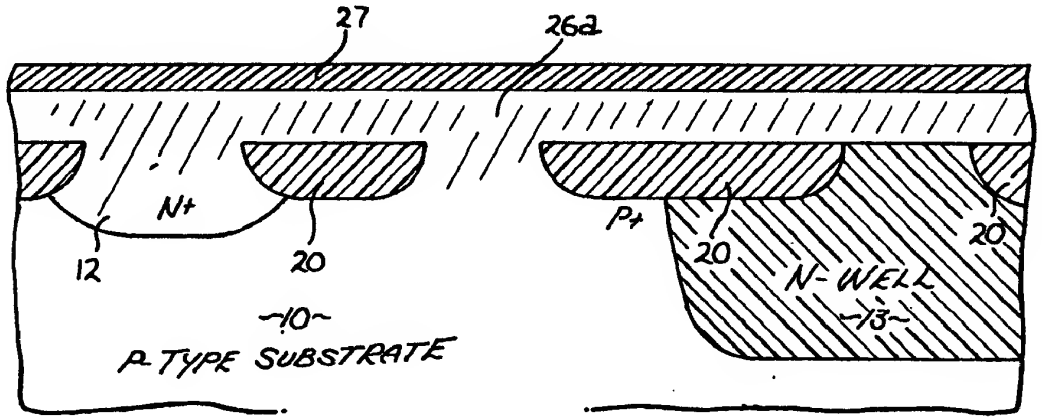

Fig. 6

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Fig. 1

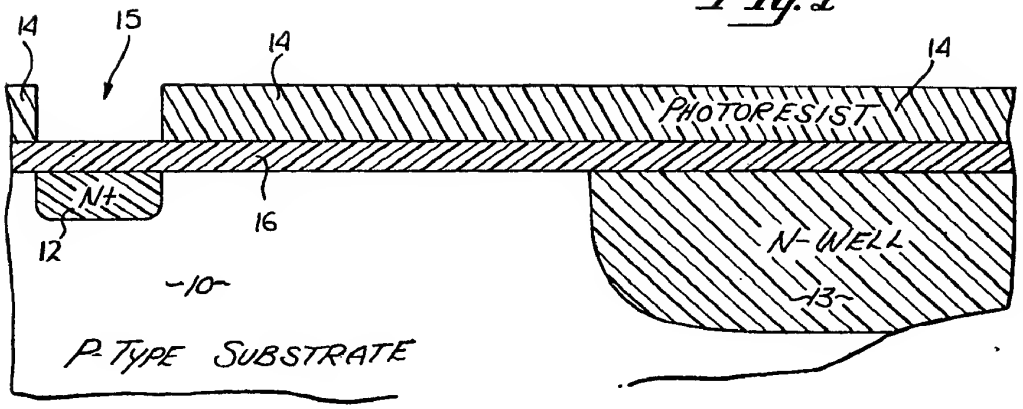
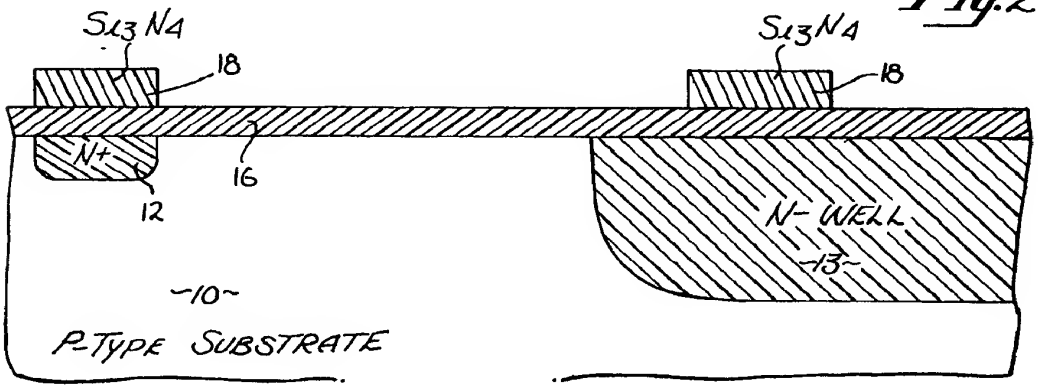


Fig. 2



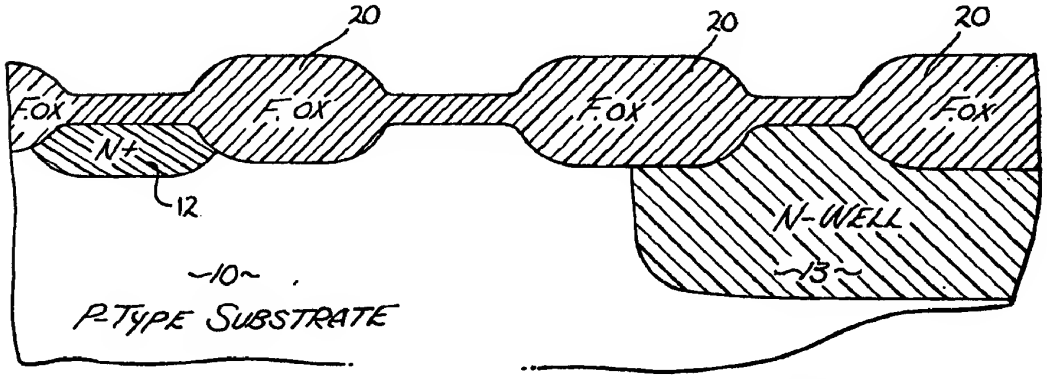


Fig. 3

Fig. 4

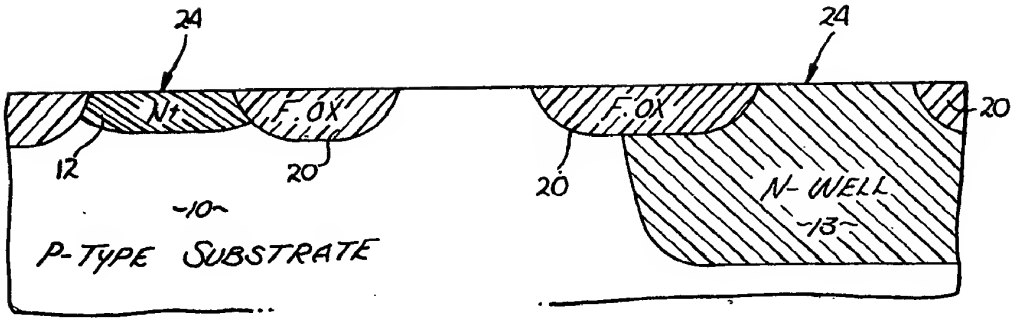
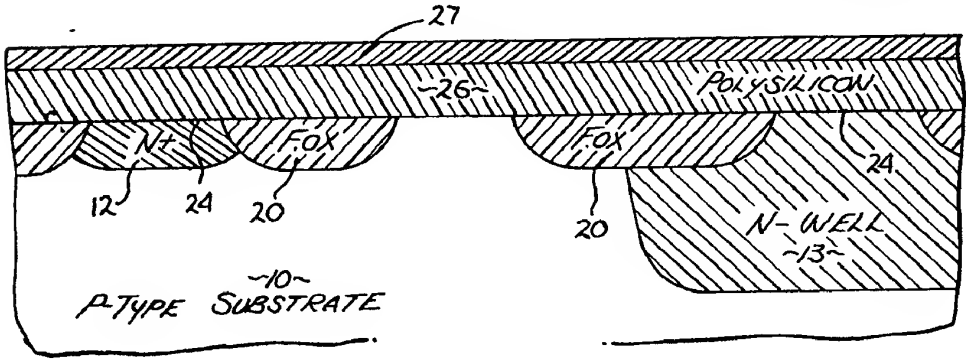


Fig. 5



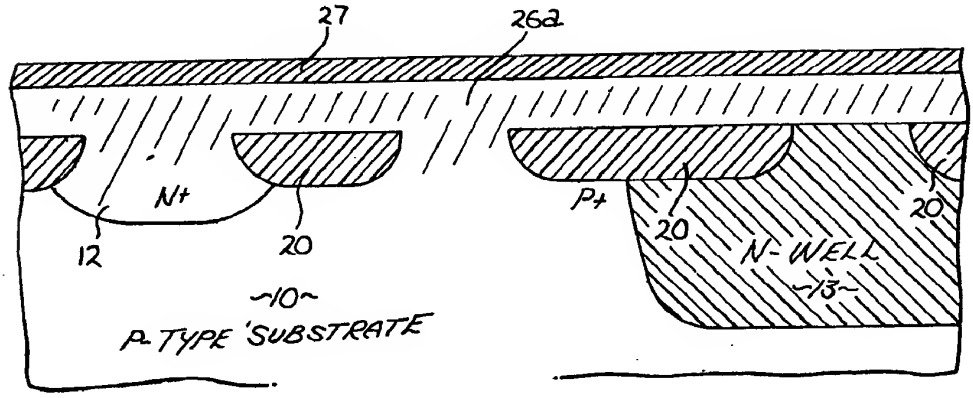


Fig. 6

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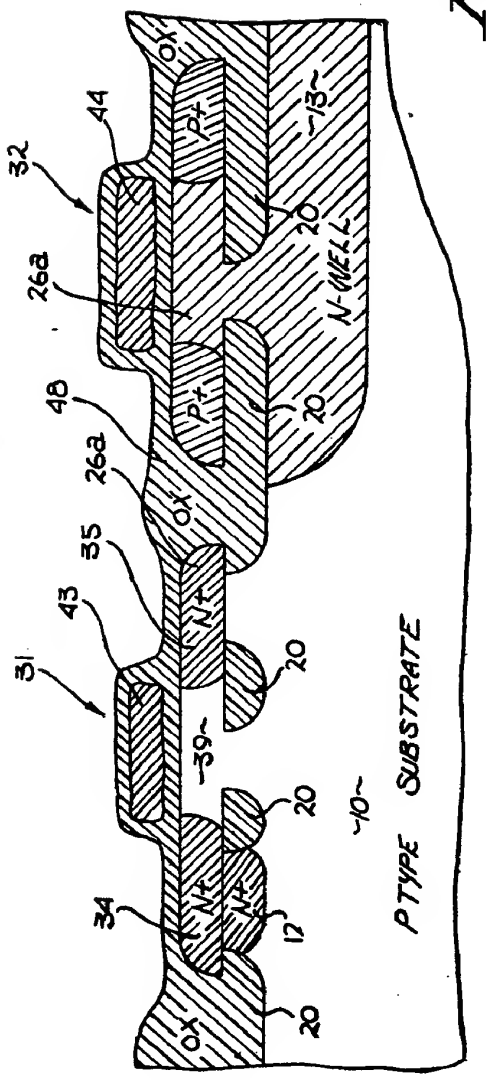

Fig. 7

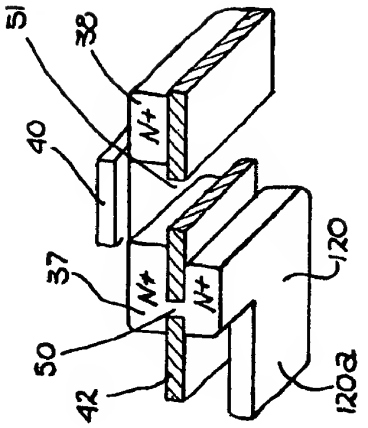

Fig. 8

SPECIFICATION

Buried interconnect for silicon on insulator structure

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The invention relates to the field of MOS integrated circuits, particularly those employing silicon on insulators.

2. Prior Art.

The present application describes an improvement in a process where an epitaxial-like layer is formed over an insulative layer. The improvement of the present application results in the formation of an interconnect in the substrate.

A process for forming an epitaxial-like layer over an insulator is described in copending application, Serial No. 700,607, filed February 11, 1985, entitled PROCESS FOR FORMING ISOLATED SILICON REGIONS AND FIELD-EFFECT DEVICES ON A SILICON SUBSTRATE, assigned to the assignee of the present invention. In the process described in this application, an insulative layer is formed on a silicon substrate and openings are formed through this layer. A polysilicon layer is then deposited over the insulative layer and contacts the substrate through the openings. Various process steps are described for recrystallizing the polysilicon layer by propagating the crystalline structure of the substrate through the openings into the polysilicon layer. Relatively high quality monocrystalline silicon is formed above the seed windows through which the recrystallization occurs. These regions are used for channel regions of MOS field-effect devices. The source and drain region for these devices are formed in the recrystallized polysilicon layer adjacent to the seed windows and over the insulation; thus the source and drain regions are isolated from the substrate.

Sections of this process are described in conjunction with the present invention since the interconnect formed with the present invention is, in its currently preferred embodiment, integrated into the process described in this application.

It is well-known to form interconnects in the substrate during the fabrication of MOS devices. These Interconnects are sometimes referred to as crossunders and often the dopant from a polysilicon layer is driven into the substrate to form the crossunders. Interconnects or crossunders formed in the substrate are described in U.S. Patent Nos. 4,013,489 and 3,964,092. In these processes, the substrate itself is part of the active circuit devices. With the silicon on insulation circuits, there is an attempt to separate the active circuit from the substrate. The present invention describes a process for forming the interconnect in the substrate where the active devices themselves are formed above the insulative layer in a recrystallized layer.

SUMMARY OF THE INVENTION

The present invention describes an improvement in a process which forms a semiconductor layer over an insulative layer where the insulative layer is formed over a silicon substrate. More particularly, the semiconductor layer such as polycrystalline silicon (polysilicon), is recrystallized by propagation of the crystalline structure of the silicon substrate through openings in the insulative layer. Devices such as MOS field-effect devices are formed in the semiconductor layer and are insulated from the substrate by the insulative layer. The improvement of the present invention comprises the formation of an interconnect within the substrate itself which provides interconnections between devices in the overlying semiconductor layer. A doped region is formed in the substrate prior to depositing the semiconductor layer over the insulative layer. An opening is formed through the insulative layer over at least a portion of this doped region, allowing the doped region to contact the semiconductor layer. The semiconductor layer is recrystallized through this opening, thereby connecting the crossunder with, for example, a source or drain region in the recrystallized layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional elevation view of a portion of a substrate which shows an n-well and a doped region formed in the substrate.

Figure 2 illustrates the substrate of Figure 1 after silicon nitride members have been formed on the substrate.

Figure 3 illustrates the substrate of Figure 2 after the growth of field oxide regions.

Figure 4 illustrates the substrate of Figure 3 after a planarization step.

Figure 5 illustrates the substrate of Figure 4 after a polysilicon layer has been formed over the substrate.

Figure 6 illustrates the substrate of Figure 5 after recrystallization of the polysilicon layer.

Figure 7 is a cross-sectional elevation view showing a larger portion of the substrate of Figure 6 after devices have been formed in the recrystallized polysilicon layer.

Figure 8 is a perspective cut-away view of a crossunder fabricated in accordance with the present invention along with an overlying device formed in the recrystallized layer.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Improved processing is described for forming an interconnect in an integrated circuit structur where the integrated circuit Is fabricated in a recrystallized semiconductor layer formed on an insulative layer. In the following

description, numerous specific details are set forth, such as specific conductivity typ s, etc., in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps have not been set forth in detail in order not to unnecessarily obscure the present invention.

As mentioned, the present invention is an improvement on processing described in co-pending application, Serial No. 700,607, filed February 11, 1985, entitled process for Forming Isolated Silicon Regions and Field-Effect Devices on a Silicon Substrate, assigned to the assignee of the present invention. The application discussed specific details on certain steps in the present invention. Reference to this prior application in the present application is made as "prior application". As described later, the present invention can also be used without the recrystallization of the prior application.

The invented process is currently preferred for the fabrication of complementary metal-oxide-semiconductor (CMOS) integrated circuits. Thus, in the following description, reference is made to regions (such as wells) used to form a particular conductivity type field-effect device. Again, it will be obvious to one skilled in the art that the present invention may be used with other technologies.

Referring now to Figure 1, a p-type monocrystalline silicon substrate 10 is shown which includes an n-well 13. As will be seen, the n-well is used, in part, for the fabrication of the p-channel devices of an integrated circuit. The substrate 10 includes a silicon dioxide layer 16 which covers the entire surface of the substrate. A photoresist layer 14 is formed on the surface and an opening 15 is shown through this layer. The opening 15 is defined at those regions where an interconnect formed in accordance with the present invention is desired. A doped region is formed in the substrate in alignment with the opening 15 as shown by region 12. It is this region which becomes the interconnect or crossunder for the integrated circuit. Thus, this region may be an elongated region or a geometrically complex region. An ordinary ion implantation step may be used to form the region 12 where the ions are implanted through the silicon dioxide layer 16. Alternately, the silicon dioxide layer 16 may be etched in alignment with opening 15 and an ordinary diffusion step used to form the d ped region 12. The photoresist layer 14 is now removed.

Next a silicon nitride layer is formed ver the substrate and patterned using rdinary masking steps to f rm the masking members 18 shown in Figure 2. One of these members is formed over the doped region 12. The silicon nitride member 18 formed ver region 12 may be formed over the entire doped region 12 or over only portions of the region 12. (It is possible to have the region 12 crossunder subsequently grown field oxide regions.) In general, the members 18 are formed over the region 12 at those sites where it is proposed for the interconnect to connect with the subsequently formed overlying integrated circuit. The other masking members 18 shown in Figure 2 are at sites of proposed channels of field-effect transistors in accordance with the teachings of the prior application.

Relatively thick field oxide regions (silicon dioxide) are now grown with the silicon nitride masking members in place. As shown in Figure 3, the field oxide regions 20 grow on the surface of the substrate where protection is not provided by the silicon nitride members. Note that the region 12 has a field oxide region disposed on both sides of region 12.

In the presently preferred processing, a planarization step is now used following the removal of the silicon nitride members to planarize the surface of the substrate as shown in Figure 4. The planarization is described in more detail in the prior application. This planarization and/or separate etching steps are used to form openings 24 which expose the substrate. Generally, these openings are formed at the sites of the previously removed silicon nitride members 18. These openings 24 of Figure 4 thus are typically aligned with the silicon nitride members 18 of Figure 2. This planarization step is not necessary to the present invention. Importantly, there is an opening above the doped region 12.

A polysilicon layer 26 is now deposited over the substrate; it contacts the doped region 12 at opening 24 as illustrated in Figure 5. A protective silicon dioxide layer 27 is also formed on the exposed surface of layer 26.

Now the layer 26 is recrystallized, causing this layer to take on the crystalline structure of the substrate. This can be accomplished by subjecting the substrate to heat from such sources as a scanning laser (e.g., CW argon laser), scanning electron beam or graphite strip heater. The openings 24 act as seed windows allowing the crystalline structure of the substrate to propagate or grow into layer 20. The layer 26 thus becomes an epitaxial-like layer shown as layer 26a in Figure 6. This recrystallization is also described in the prior application.

While in the preferred embodiment recrystallization of the polysilicon layer is used, the interconnect of the present invention can be formed even where no recrystallization occurs, for instance, where transistors are formed in the polysilicon layer.

In Figure 7, a wider view of the substrate is shown after field-effect devices have been formed in the recrystallized layer 26a. An n-type transistor 31 having a polycrystalline silicon gate 43 and sourc and drain regions 34

and 35 is shown formed above one of the seed windows. The channel 39 of this transistor is formed directly above th seed window, and as described in the prior application, the highest quality monocrystalline silicon occurs at these seed windows. The region 34 of this transistor is coupled directly to region 12. Thus, one terminal of this transistor may be interconnected with another device formed in the recrystallized layer 26a. Note that the insulative regions 20 cause a relatively long conductive path to be formed between the channel 39 of transistor 31 and well 13, thus reducing possible latch up. Another transistor 32 is also shown formed above the n-well 13. This p-type transistor includes a gate 44.

Transistors 31 and 32 are isolated from one another in the recrystallized layer by oxide region 48. The formation of this region is described in the prior application.

In Figure 8, a transistor is shown formed in a recrystallized layer as described above. The source and drain regions 37 and 38 are formed on the insulative layer 42. The seed window 51 is open in this view. This region is typically the channel of the transistor as mentioned; a gate 40 overlies this channel. Another opening 50 through layer 42 includes the interconnect of the present invention. As can be seen in this view, the doped region 120 extends in two directions. That is, region 120a extends perpendicular to regions 37 and 38, and to the portion of region 120 underlying region 37. The doped region 120 may provide a common connection between several devices in the recrystallized layer.

Thus, an improvement in a process where integrated circuits are formed in a recrystallized polysilicon layer formed on an insulation is disclosed. In particular, an interconnect formed within the substrate forms the connection between devices in the recrystallized layer.

CLAIMS

1. In a process for forming a semiconductor layer over an insulative layer where said insulative layer is formed over a substrate and said semiconductor layer is formed over said insulative layer, and where devices are formed in said semiconductor layer, an improvement for forming an interconnect in said substrate for sald devices comprising the steps of:

forming a doped region in said substrate prior to depositing said semiconductor layer on said insulative layer;

forming an opening through said insulative layer over said doped region;

forming said semiconductor layer at said opening over said doped r gion,

whereby said doped reglon forms an interconnect for said devices.

2. In a process for forming a semiconductor layer over an insulative layer where said insulative layer is formed over a substrate and said semiconductor layer is recrystallized through a plurality of openings in said insulative layer allowing the crystalline structure of said substrate to propagate into said semiconductor layer, and where devices are formed in said semiconductor layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming an elongated doped region in said substrate prior to depositing said semiconductor layer on said insulative layer;

forming a doped region in said substrate prior to depositing said semiconductor layer on said insulative layer;

forming an opening through said insulative layer over said doped region;

recrystallizing said semiconductor layer at said opening over said doped region,

whereby said doped region forms an interconnect for said devices.

3. In a process for forming a semiconductor layer over an insulative layer where said insulative layer is formed over a substrate and said semiconductor layer is recrystallized through a plurality of openings in said insulative layer allowing the crystalline structure of said substrate to propagate into said semiconductor layer, and where devices are formed in said semiconductor layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming a doped region in said substrate prior to the deposition of said semiconductor layer on said insulative layer;

depositing said semiconductor layer such that said layer contacts said doped region through an opening in said insulative layer;

recrystallizing said semiconductor layer at said opening over said doped region,

whereby said doped region forms an interconnect for said devices.

4. In a process for forming a semiconductor layer over an insulative layer where said insulative layer is formed over a substrate and said semiconductor layer is recrystallized through a plurality of openings in said insulative layer allowing the crystalline structure of said substrate to propagate into said semiconductor layer, and where devices are formed in said semiconductor layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming a doped region in said substrate prior to the deposition of said semiconductor layer on said insulative layer;

forming a silicon nitride member over at least a portion of said doped region;

growing field oxide regions with said silicon nitride member in place;

removing said silicon nitride member;

depositing said semiconductor layer over said insulative layer such that said semiconductor layer contacts said doped region through an opening in said insulative layer located at the site of said removed silic n ni-

tride member;

recrystallizing said semiconductor layer through said opening,

whereby said doped region forms an interconnect for said devices.

5. The improvement defined by Claim 4 including a planarization step to planarize the surface of said substrate following said step of growing said field oxide regions.

6. In a process for forming an epitaxial-like silicon layer from a polysilicon layer where a polysilicon layer is formed over a silicon dioxide layer and said silicon dioxide layer is formed over a silicon substrate, said process including the recrystallization of said polysilicon layer through a plurality of openings in said silicon dioxide layer allowing the crystalline structure of said silicon substrate to propagate into said polysilicon layer to form said epitaxial-like layer, and where devices are formed in said epitaxial-like layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming a doped region in said substrate prior to depositing said polysilicon layer on said silicon dioxide layer;

forming an opening through said silicon dioxide layer over said doped region;

depositing said polysilicon layer;

recrystallizing said polysilicon layer through said opening,

whereby said doped region forms an interconnect for said devices.

7. In a process for forming an epitaxial-like silicon layer from a polysilicon layer where the polysilicon layer is formed over an silicon dioxide layer and said silicon dioxide layer is formed over a silicon substrate, said process including the recrystallization of said polysilicon layer through a plurality of openings in said silicon dioxide layer allowing the crystalline structure of said silicon substrate to propagate into said polysilicon layer to form said epitaxial-like layer, and where devices are formed in said epitaxial-like layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming a doped region in said substrate prior to deposition of said polysilicon layer on silicon dioxide layer;

depositing said polysilicon layer such that polysilicon layer contacts said doped region through an opening in said insulative layer;

recrystallizing said polysilicon layer through said opening,

whereby said doped region forms an interconnect for said devices.

8. Th improvement defined in Claim 7 wherein said doped region contacts one f a source and drain regions of one of said devices.

9. In a process for forming an epitaxial-like silic n layer from a polysilicon layer where the polysilicon layer is formed over an silicon dioxide layer and said silicon dioxide layer is formed over a silicon substrate, said process including the recrystallization of said polysilicon layer through a plurality of openings in said silicon dioxide layer allowing the crystalline structure of said silicon substrate to propagate into said polysilicon layer to form said epitaxial-like layer, and where devices are formed in said epitaxial-like layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming an elongated doped region in said suhstrate prior to depositing said polysilicon layer on said silicon dioxide layer;

forming an opening through said silicon dioxide layer over said doped region;

depositing said polysilicon layer;

recrystallizing said polysilicon layer through said opening,

whereby said doped region forms an interconnect for said devices.

10. The improvement defined in Claim 9 wherein said doped region contacts one of a source and drain regions of one of said devices.

11. In a process for forming an epitaxial-like silicon layer from a polysilicon layer where the polysilicon layer is formed over an silicon dioxide layer and said silicon dioxide layer is formed over a silicon substrate, said process including the recrystallization of said polysilicon layer through a plurality of openings in said silicon dioxide layer allowing the crystalline structure of said silicon substrate to propagate into said polysilicon layer to form said epitaxial-like layer, and where devices are formed in said epitaxial-like layer, an improvement for forming an interconnect in said substrate for said devices comprising the steps of:

forming a doped region in said substrate prior to depositing said polysilicon layer on said silicon dioxide layer;

forming a silicon nitride member over at least a portion of said doped region;

growing field oxide regions with said silicon nitride member in place;

removing said silicon nitride member;

depositing said polysilicon layer over said insulative layer such that said polysilicon layer contacts said doped region at the site of said removed silicon nitride member;

recrystallizing said polysilicon layer above said doped region;

forming said devices on substrate such that said doped region is in electrical contact with at least some of said devices,

whereby said doped region forms an Interconnect for said devices.

12. The improvement defined by Claim 11 including the step f planarizing the surface of said substrate followlng sald growth of said field oxide regions.

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